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06EC45

Fourth Semester B.E. Degree Examination, Dec.2013/Jan.2014
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Compare VHDL and Verilog. **(06 Marks)**

b. What are values that std-logic (VHDL) and nets (verilog) can take? **(06 Marks)**

c. With proper example explain the logical operators of verilog. **(08 Marks)**

2 a. What are the facts of data flow description? **(02 Marks)**

b. Starting from the basics draw the logic symbol of D'latch excitation table, K map circuit for D latch and write VHDL and verilog program for the same. **(10 Marks)**

c. Write a data flow description (in both VHDL and verilog) of a full adder with enable. If the enable is low (0), the sum and carry are zero; otherwise the sum and carry are usual outputs of the adder. Use a 5 ns delay for any gate including xor. Draw the truth table of this adder and derive the Boolean function after minimization. **(08 Marks)**

3 a. With syntax explain different types of loops in VHDL and verilog. **(10 Marks)**

b. Write a program in VHDL and verilog for JK flip flop using if & else if statements. **(10 Marks)**

4 a. What is binding? Explain the binding between entity and components in VHDL and between two modules in verilog. **(10 Marks)**

b. Write VHDL behavioral description of a tristate buffer. Use this as a component for structural of 2 to 4 decoder with tristate output. **(10 Marks)**

PART – B

5 a. Write VHDL procedure and verilog task for N-bit ripple carry adder. **(10 Marks)**

b. With suitable example write VHDL code for writing integers to a file. **(10 Marks)**

6 a. Give an example of a VHDL package. **(08 Marks)**

b. Write the block diagram and function table of a SRAM of 16×8 and write verilog code for the same. **(12 Marks)**

7 a. How to invoke a verilog module from a VHDL module? Giving an example of a full adder using two half adders. **(10 Marks)**

b. Discuss the facts and limitations of mixed language description. **(10 Marks)**

8 a. Draw the flow chart and explain the steps involved in synthesis. **(10 Marks)**

b. Write a program in VHDL and obtain the gate level synthesis for BP and ADH. BP is the input and ADH is the output. BP varies from 0 to 7 and ADH varies from 0 to 16. Assume that if BP is more than 5 the ADH is 0. For BP > 2 and less than 5 the ADH is given by ADH = – 5*BP + 25 **(10 Marks)**

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